# Lab Report 3

## Materials:

Logic Box, Gates –AND, OR, Exclusive OR, wire.

## Method:

1. Build each of the circuits shown below.
2. Connect the inputs to the switches on the logic boxes labeled below.
3. Connect the output to the LED.
4. Record the truth table results for each part.



**Circuit 1: Half Adder**



**Circuit 2: Full Adder**

## Results:

|  |  |  |  |
| --- | --- | --- | --- |
| **Input** | | **Output** | |
| **S1** | **So** | **Sum - LO** | **Carry Out – L1** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| **Circuit 1: Half Adder** | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input** | | | **Output** | |
| **S2** | **S1** | **S0** | **Sum - LO** | **Carry Out – L1** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** |
| **Circuit 2: Full Adder** | | | | |

## Conclusion:

* **Circuit 1:**
* **The output of sum is high when the input is 1 and not the other. This is equal to XOR Gate.**
* **The output of carry out is high when both of the inputs are high. This is equal to AND Gate.**
* **In theory, the output corresponds with the lab results.**
* **Circuit 2:**
* **The output for sum is high when 1, 2 or all of the inputs are high.**
* **The output for carry out is high 2 or more inputs are high.**
* **In theory, the output corresponds with the lab results.**

In conclusion, we can say that both of the adders work as expected. The difference between a half adder and a full adder is Half Adder doesn’t have Carry in, whereas Full Adder has a Carry in. The half-adder accepts two binary digits on its inputs and produces two binary digits on its outputs, a sum bit and a carry bit. We also can establish according to the logic gates drawings & Boolean expressions ‘Two Half-Adders make a Full-Adder with both of the outputs ORed together.’